WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a sense amplifier;

first and second word lines;

first and second bit lines coupled to said sense amplifier;

a first memory cell coupled to said first word line and said first bit line; and

a second memory cell coupled to said second word line and said second bit line;

wherein, in a normal mode, the first and second word lines are assigned separate addresses from each other, and data access operation is performed in the first and second memory cells separately;

whereas in a partial mode, the first and second word lines are assigned the same address to maintain one bit data in the first and second memory cells;

wherein, in order to copy a data in the first memory cell into the second memory cell, based on a switching from the normal mode to the partial mode,

the second word line is activated in a precharge period for the first and second bit lines, so that a precharge voltage is written into the second memory cell;

then, the first word line is activated; and

then, the sense amplifier is activated to amplify a differential voltage between the first and second bit lines to store said data stored in said first memory cell into said memory cell.

2. The device as claimed in claim 1, further comprising:

a trigger signal generator which generates a refresh trigger signal to control a refresh operation of said first and second memory cells, when the copying is entry, said trigger signal generator generating said refresh trigger signal at a first period which is the same as a period of said refresh trigger signal generated at a period of said normal mode, then, said trigger signal generator generating said refresh trigger signal at a second period which is longer than said first period.

3. A semiconductor memory device, comprising:

a sense amplifier;

first and second word lines;

first and second bit lines coupled to said sense amplifier;

a first memory cell coupled to said first word line and said first bit line; and

a second memory cell coupled to said second word line and said second bit line;

wherein, in a normal mode, the first and second word lines are assigned separate addresses from each other, and data access operation is performed in the first and second memory cells separately;

whereas in a partial mode, the first and second word lines are assigned the same address to maintain one bit data in the first and second memory cells; and

wherein, in order to copy a data in the first memory cell into the second memory cell, based on a switching from the normal

mode to the partial mode,

the first word line is activated;

then, the sense amplifier is activated to amplify a differential voltage between the first and second bit lines; and

the second word line is activated, thereby storing said data stored in said first memory cell into said memory cell;

when said copying is operated, said first word line is activated at a first activate period, said second word line is activated at a second active period which is shorter than said first active period.

4. The device as claimed in claim 3, wherein

said first activate period is the same as that of said first word line in said normal mode.

5. The device as claimed in claim 3, wherein

said second activate period is the same as that of said first word line in said normal mode.

6. The device as claimed in claim 5, wherein

if a read/write access occurs at a time after the first word line is activated but before the second word line is activated during said partial mode, the first word line is activated for the same period of time as the period of activating in the normal mode and is thereafter inactivated, and activation of the second word line is interrupted so that a read/write operation is performed.

7. The device according to claim 6, wherein if a read/write access occurs while the first word line is being activated and after the second word line is activated during said partial mode, the first word line is activated for a longer period than the period of activating in the normal mode, the second word line is activated for the same period as the activation period in the normal mode, and then a read/write operation is performed.

8. The device according to claim 1, further comprising:

a timer to generate a trigger signal;

a delay circuit for delaying the trigger signal;

a first pulse-generating circuit for generating a first one-shot pulse based on the output of the delay circuit;

a first word driver which receives said first one-shot pulse to drive said first word line; and

a second pulse-generating circuit for generating a second one-shot pulse based on the trigger signal;

a selector circuit which receives said first and second one-shot pulses to output a selected one-shot pulse; and

a second word driver which receives said selected one-shot pulse to drive the second word line.

9. The device according to claim 8, wherein:

said timer generates said trigger signal with a first cycle and a second cycle which is different from said first cycle

10. The device according to claim 9, wherein:

said timer generates said trigger signal with said first cycle when said copy is performed and generates said trigger signal with said second cycle after said trigger signal with said first cycle is generated.

11. The device according to claim 10, wherein

said first cycle is the same period as a cycle with when said timer generates said trigger signal in said normal mode, said second cycle has a period which is longer than that of said first cycle.

12. The device according to claim 10, wherein

said first cycle has a period which is shorter than that of a cycle with when said timer generates said trigger signal in said normal mode, said second cycle has a period which is longer than that of said cycle with when said timer generates said trigger signal in said normal mode.

13. The device according to claim 3, further comprising:

a refresh timer which generates a trigger signal;

a frequency dividing circuit for dividing frequency of the trigger signal;

a logic gate for performing a logical operation between a chip select signal and a control signal for controlling the normal mode and the partial mode;

a refresh cycle period-determining circuit for, based on an output signal from the logic gate, determining a cycle period of the trigger signal to be said first cycle period and then

to be a second cycle period longer than that of said first cycle when the control signal indicates the partial mode and the chip select signal is in an inactivated state, and determining the cycle period of the trigger signal to be said first cycle period when the chip select signal is in an activated state; and

a selector circuit for selecting an output signal from the refresh timer when said determining circuit produces said trigger signal with said first cycle and selecting a frequency division signal from the frequency dividing circuit when said determining circuit produces said trigger signal with said second cycle.

14. The semiconductor memory device according to claim 13, further comprising:

a circuit for generating a control signal for controlling precharge of the bit lines and activation of the sense amplifier based on the trigger signal output from the selector circuit, an output signal from the refresh cycle period-determining circuit, and an output signal from the logic gate;

a pulse generator for generating one-shot pulse, being a core activating pulse, for controlling activation of the cell array based on the trigger signal or detection of change of an address supplied from outside of the semiconductor memory device;

a first logic gate for supplying an output of a first predetermined result of a logical operation between the core activating pulse and the control signal that controls the precharge and the activation of the sense amplifier to a circuit for precharging the bit lines; and

a second logic gate for supplying, as a sense amplifier-activating signal, an output of a second predetermined result of the logical operation between the core activating pulse and the signal that controls the precharge and the activation of the sense amplifier to the sense amplifier.

15. The semiconductor memory device according to claim 13, further comprising:

a refresh address generator for generating a refresh address signal based on the trigger signal output from the selector circuit;

a first control circuit for generating a predetermined bit signal and an inverted signal of the predetermined bit signal based on a predetermined bit signal of the refresh address signal that is output from the refresh address generator, an output signal from the refresh cycle period-determining circuit, and output signals from the logic gates; and

a second control circuit for controlling activation of the first and second word lines based on, at least, the predetermined bit signal, the inverted signal of the predetermined bit signal, and an address signal corresponding to the first word line.

16. A semiconductor memory device, comprising:

a sense amplifier;

first and second bit lines commonly coupled to said sense amplifier;

first and second memory cells coupled to said first and

second bit lines; and respectively, said first and second memory cells that stores and holds one bit data complementarily; wherein

when copying a data stored in one of the first and second memory cells into the other one of the memory cells,

a data in the other one of the memory cells is reset;

after the resetting, a word line connected to the one of the memory cells is activated;

after the activation, the data on the bit line read out from the one of the cells is amplified by said sense amplifier on said first and second bit lines; and

after amplified, the data is stored in the other memory cell.

17. The device according to claim 16, wherein said reset is performed by an operation such that a word line connected to the other one of the memory cells in a precharge period for bit lines.

18. A method of controlling a semiconductor memory device that stores and holds one bit of data complementarily by two memory cells respectively connected to two bit lines, which form a bit line pair, commonly connected to one sense amplifier, the method comprising the steps of:

resetting, when copying a cell data of one of the two memory cells into the other one of the memory cells, a cell data of the other one of the memory cells that is a copy destination; and

activating, after resetting the other one of the memory

cells, a word line connected to the one of the memory cells, amplifying by the sense amplifier the data of the one of the memory cells to be output to the bit line pair, and storing the cell data of the one of the memory cells into the other one of the memory cells from the sense amplifier via the bit line pair.

19. The method of controlling a semiconductor memory device according to claim 18, wherein the step of resetting the cell data of the other one of the memory cells comprises a step of writing an intermediate voltage into the other one of the memory cells by activating a word line connected to the other one of the memory cells in a period in which the bit line pair is precharged to a precharge voltage being an intermediate voltage between a high-potential side power supply voltage and a low-potential side power supply voltage.

20. The method of controlling a semiconductor memory device according to claim 19, wherein:

the two memory cells are respectively connected to two word lines;

in a normal mode, the two word lines are assigned separate addresses; and

in a twin cell mode in which one bit of data is complimentarily stored and held by the two memory cells, the two word lines are assigned the same address and are activated with the same timing after a cell data of one of the two memory cells has been copied into the other one of the memory cells.

21. The method of controlling a semiconductor memory device according to claim 20, wherein the copy operation of a data of one of the two memory cells into the other one of the memory cells is performed based on a trigger signal for instructing a refresh operation of dynamic type memory cells.